



AK100 Datasheet

Features :

- Philips's LPC2104 ARM chip with on-chip 128K bytes Flash and 16K bytes SRAM.
- High performance with speed up to 60MHz.
- On-board USB circuit for communication and power supplying with ARMKEY board stand-alone.
- Generating all the powers needed within ARMKEY board.
- Two-wire serial EEPROM for specific USB-ID and user's data holding.
- Pin-compatible DIP-40 package with 8051 microcontroller.
- Three configuration modes with LPC2104 ARM chip : ISP, IAP and JTAG.
- Voltage detection IC for the valid reset signal.
- On-board reset switch.
- LPC210X eForth system for application developing on-board.
- Third-party development tools and software support possibly.

Description

The ARMKEY is a system on a board module, housed in a DIP-40 package. It uses a high performance and low power consumption ARM chip as like a main control unit. This chip can speed up to 60MHz via internal on-chip PLL. There are 32 general purpose input/output pins at most, each pin can be multiplex with on-chip peripheral specific function pin. This ARM chip has many on-chip peripheral units : including two Capture/Compare/ Timers, a 32-bits GPIO, a PWM, a RTC, a IIC serial interface, a SPI serial interface, two UARTs, a Watch-Dog Timer and a system control unit. For the on-chip memory, it includes 128K bytes Flash and 16K~64K bytes SRAM. There are many kinds of chip configuration modes could be used : including ISP, IAP and JTAG.

There are a USB chip for communicating and power-supplying to the module stand alone. It can easily use Windows' hyper-terminal to developing any application with this module in an interactive mode real-time. An additional serial EEPROM is option for setting customer's USB-ID or holding private data.

For other special design in this module, it uses an 8051-compatible pin assignment for replace any exist 8051 application easily. It lets you have 8051's functions and have ARM's high performance.



Pin Assignment

P0.0/TxD0/PWM1	1		40	VCC
P0.1/RxD0/PWM3	2		39	P0.31/EXTIN0/STDO
P0.2/SCL/CAP0.0	3		38	P0.30/TRACEPKT3/STDI
P0.3/SDA/MAT0.0	4		37	P0.29/TRACEPKT2/STCK
P0.4/SCK/CAP0.1	5		36	P0.28/TRACEPKT1/STMS
P0.5/MISO/MAT0.1	6		35	P0.27TRACEPKT0/STRST
P0.6/MOSI/CAP0.2	7		34	P0.26/TRACESYNC
P0.7/SSEL/PWM2	8		33	P0.25/PIPESTAT2
nRESET	9		32	P0.24/PIPESTAT1
P0.8/TxD1/PWM4	10		31	AIN
P0.9/RxD1/PWM6	11		30	BTCK
P0.10/RTS1/CAP1.0	12		29	DBGSEL
P0.11/CTS1/CAP1.1	13		28	P0.23/PIPESTAT0
P0.12/DSR1/MAT1.0	14		27	P0.22/TRACECLK
P0.13/DTR1/MAT1.1	15		26	P0.21/PWM5/PTDO
P0.14/DCD1/EINT1	16		25	P0.20/MAT1.3/PTDI
P0.15/RI1/MAT0.2	17		24	P0.19/MAT1.2/PTCK
5V0	18		23	P0.18/CAP1.3/PTMS
3.3V0	19		22	P0.17/CAP1.2/PTRST
GND	20		21	P0.16/EINT0/MAT0.2

Pin Description

Pin NO.	Name	I/O Type	Function
1	P0.0	I/O	Port 0 bit 0.
	TxD0	O	UART0 Transmitter output.
	PWM1	O	Pulse Width Modulator output 1.
2	P0.1	I/O	Port 0 bit 1.
	RxD0	I	UART0 Receiver input.
	PWM3	O	Pulse Width Modulator output 3.
3	P0.2	I/O	Port 0 bit 2.
	SCL	OD	I2C clock signal.
	CAP0.0	I	Capture input for Timer0, channel 0.
4	P0.3	I/O	Port 0 bit 3.
	SDA	OD	I2C data signal.



	MAT0.0	O	Match output for Timer0, channel 0.
5	P0.4	I/O	Port 0 bit 4.
	SCK	I/O	Master Output Slave Input. SPI clock signal.
	CAP0.1	I	Capture input for Timer0, channel 1.
6	P0.5	I/O	Port 0 bit 5.
	MISO	I/O	Master In Slave Out. SPI data signal.
	MAT0.1	O	Match output for Timer0, channel 1.
7	P0.6	I/O	Port 0 bit 6.
	MOSI	I/O	Master Out Slave In. SPI data signal.
	CAP0.2	O	Capture input for Timer0, channel 2.
8	P0.7	I/O	Port 0 bit 7.
	SSEL	I	Slave Select.
	PWM2	O	Pulse Width Modulator output 2.
9	nRESET	I	Main Reset input.
10	P0.8	I/O	Port 0 bit 8.
	TxD1	O	UART1 Transmitter output.
	PWM4	O	Pulse Width Modulator output 4.
11	P0.9	I/O	Port 0 bit 9.
	RxD1	I	UART1 Receiver input.
	PWM6	O	Pulse Width Modulator output 6.
12	P0.10	I/O	Port 0 bit 10.
	RTS1	O	UART1 Request to Send output.
	CAP1.0	O	Capture input for Timer1, channel 0.
13	P0.11	I/O	Port 0 bit 11.
	CTS1	I	UART1 Clear to Send input.
	CAP1.1	O	Capture input for Timer1, channel 1.
14	P0.12	I/O	Port 0 bit 12.
	DSR1	I	UART1 Data Send Ready input.
	MAT1.0	O	Match output for Timer1, channel 0.
15	P0.13	I/O	Port 0 bit 13.
	DTR1	O	UART1 Data Terminal Ready output.
	MAT1.1	O	Match output for Timer1, channel 1.
16	P0.14	I/O	Port 0 bit 14.
	DCD1	I	UART1 Data Carrier Detect input.
	EINT1	I	External interrupt input 1.
17	P0.15	I/O	Port 0 bit 15.
	RI1	I	UART1 Ring Indicator input.
	EINT2	I	External interrupt input 2.



18	5VO	O	5V Power Output.
19	3.3VO	O	3.3V Power Output.
20	GND	I	Ground
21	P0.16	I/O	Port 0 bit 16.
	EINT0	I	External interrupt input 0.
	MAT0.2	O	Match output for Timer0, channel 2.
22	P0.17	I/O	Port 0 bit 17.
	CAP1.2	I	Capture input for Timer1, channel 2.
	PTRST	I	Primary JTAG test reset input.
23	P0.18	I/O	Port 0 bit 18.
	CAP1.3	I	Capture input for Timer1, channel 3.
	PTMS	I	Primary JTAG test mode select input.
24	P0.19	I/O	Port 0 bit 19.
	MAT1.2	O	Match output for Timer1, channel 2.
	PTCK	I	Primary JTAG test clock input.
25	P0.20	I/O	Port 0 bit 20.
	MAT1.3	O	Match output for Timer1, channel 3.
	PTDI	I	Primary JTAG test data input.
26	P0.21	I/O	Port 0 bit 21.
	PWM5	O	Pulse Width Modulator output 5.
	PTDO	O	Primary JTAG test data output.
27	P0.22	I/O	Port 0 bit 22.
	TRACECLK	O	Trace Clock. Internal pull-up.
28	P0.23	I/O	Port 0 bit 23.
	PIPESTAT0	O	Pipeline Status, bit 0. Internal pull-up.
29	DBGSEL	I	When high, debug mode is active. Otherwise, normal operation. Internal pull-up.
30	RTCK	I/O	Return Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Also used during debug mode entry to select primary or secondary JTAG pins. Internal pull-up.
31	ATN	I	Attention input to reset system.
32	P0.24	I/O	Port 0 bit 24.
	PIPESTAT1	O	Pipeline Status, bit 1. Internal pull-up.
33	P0.25	I/O	Port 0 bit 25.
	PIPESTAT2	O	Pipeline Status, bit 2. Internal pull-up.



34	P0.26 TRACESYNC	I/O O	Port 0 bit 26. Trace Synchronization. Internal pull-up.
35	P0.27 TRACEPKT0 STSRT	I/O O I	Port 0 bit 27. Trace Packet, bit 0. Internal pull-up. Secondary JTAG test reset input.
36	P0.28 TRACEPKT1 STMS	I/O O I	Port 0 bit 28. Trace Packet, bit 1. Internal pull-up. Secondary JTAG mode select input.
37	P0.29 TRACEPKT2 STCK	I/O O I	Port 0 bit 29. Trace Packet, bit 2. Internal pull-up. Secondary JTAG test clock input.
38	P0.30 TRACEPKT3 STDI	I/O O I	Port 0 bit 30. Trace Packet, bit 3. Internal pull-up. Secondary JTAG test data input.
39	P0.31 EXTIN0 STDO	I/O I I	Port 0 bit 31. External Trigger Input. Internal pull-up. Secondary JTAG test data output.
40	VCC	I	5V Power Supply Input

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